IN THE SPECIFICATION:

On page 2, at line 17, please replace "ordered" with "unordered" and on line 18 please delete the word "for" as follows:

Coherent interfaces interconnecting the I/O hub and, ultimately, to the processors, are inherently unordered. Therefore, ordering rules under the P/C model are more restrictive than those for a coherent interface, which may have no ordering rules at all. Coherent interfaces, such as a front-side bus or an Intel Scalability Port, are inherently ~~ordered~~ unordered because the processors for which the coherent interface was designed ~~for~~ are complex devices. These processors have the intelligence to distinguish when ordering is required and when it is not. Therefore, in general, coherent interfaces can treat completions independently of requests (in either direction). PCI devices, however, are generally not this complex and are more cost-sensitive, and therefore rely on the system ordering rules to avoid deadlocks. PCI ordering rules do allow some flexibility in relaxing the ordering requirements of specific transactions, though.